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1 Alpha du centaur: a prototype environment for the design of parallel regular alorithms
Pierrick Gachet, Christophe Mauras, Patrice Quinton, Yannick Saouter
June 1986 **Proceedings of the 3rd international conference on Supercomputing**
Full text available: pdf(966.30 KB) Additional Information: full citation, abstract, references, index terms

We describe Alpha du Centaur (ADC), a prototype environment for the design of parallel regular algorithms. In ADC, a program is specified using the Alpha language, using system of parameterized linear recurrence equations. The goal of ADC is to make it possible to transform the initial specifications into a parallel algorithm, that is to say, another system of recurrence equations, in which the time and the space index are separated. The first section of the paper is devoted to a ...

2 A novel method for stochastic nonlinearity analysis of a CMOS pipeline ADC
David Goren, Eliyahu Shamsaevc, A. Wagner
June 2001 **Proceedings of the 38th conference on Design automation**
Full text available: pdf(334.01 KB) Additional Information: full citation, abstract, references, index terms

An analytic appraoch is presented for estimating the nonlinearity of an analog to digital converter (ADC) as a function of the variations in the circuit devices. The approach is demonstrated for the case of a pipeline ADC with digital error correction. Under some mild assumptions on the expected variations, the error probability is expressed as a simple explicit function of the standard deviations in the components' parameters: gain errors, comparator offset errors and resistor errors. The ...

3 Power optimization using divide-and-conquer techniques for minimization of the number of operations
Inki Hong, Miodrag Potkonjak, Ramesh Karri
October 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 4
Full text available: pdf(278.45 KB) Additional Information: full citation, abstract, references, index terms

We introduce an approach for power optimization using a set of compilation and architectural techniques. The key technical innovation is a novel divide-and-conquer compilation technique to minimize the number of operations for general computations. Our technique optimizes not only a significantly wider set of computations than the previously published techniques, but also outperforms (or performs at least as well as other techniques) on all examples. Along the architectural dimension, we in ...

Keywords: code generation, transformations

4 Low power converter circuits: A low-power rail-to-rail 6-bit flash ADC based on a novel complementary average-value approach

Hui-Chin Tseng, Hsin-Hung Ou, Chi-Sheng Lin, Bin-Da Liu

August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**

Full text available: pdf(286.33 KB) Additional Information: full citation, abstract, references, index terms

In this paper, a 6-bit 300-MSample/s(MS/s) flash analog-to-digital converter (ADC) with a novel complementary average-value (CAV) approach is proposed. Input signal is pre-processed and then steered to be compared with a fixed reference voltage level, which greatly simplifies the comparator design and thus power consumption is reduced. In addition, rail-to-rail input range can be achieved by the proposed CAV technique, and the offset as well as bubble errors can therefore be minimized as a resul ...

Keywords: CMOS analog circuit, comparator, flash analog-to-digital converter, low power, rail-to-rail

5 A performance evaluation of several priority policies for parallel processing systems

Randolph Nelson, Donald Towsley

July 1993 **Journal of the ACM (JACM)**, Volume 40 Issue 3

Full text available: pdf(1.41 MB) Additional Information: full citation, references, citings, index terms

Keywords: priority scheduling, speedup

6 Power optimization using divide-and-conquer techniques for minimization of the number of operations

Inki Hong, Miodrag Potkonjak, Ramesh Karri

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(55.12 KB) Additional Information: full citation, abstract, references, citings, index terms

Publisher Site

We develop an approach to minimizing power consumption of portable wireless DSP applications using a set of compilation and architectural techniques. The key technical innovation is a novel divide-and-conquer compilation technique to minimize the number of operations for general DSP computations. Our technique optimizes not only a significantly wider set of computations than the previously published techniques, but also outperforms (or performs at least as well as other techniques) on all exampl ...

Keywords: DSP computations, architectural techniques, compilation, data flow graphs, divide-and-conquer compilation, portable wireless DSP applications, power consumption

7 Parallelism in sequential multiprocessor simulation models: a case study

Hatem Sellami, Sudhakar Yalamanchili

April 1995 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 5 Issue 2

Full text available: pdf(1.56 MB) Additional Information: full citation, abstract, references, index terms, review

The design and analysis of multiprocessor simulation models represents a complex and computationally demanding application that is a candidate for parallel simulation. This paper examines the application of conservative parallel discrete event simulation on a set of existing "real-world" models created over the years with no thought given to the parallel execution. These models are based on a subset of Petri Nets known as Marked graphs. The results of the study ...

Keywords: Petri nets, conservative synchronization, discrete event simulation, marked graphs, parallel architectures, parallel simulation, parallelism, partitioning and mapping

8 Mixed analog-digital design: Digital background and blind calibration for clock skew error in time-interleaved analog-to-digital converters

David Camarero, Jean-François Naviner, Patrick Loumeau

September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**

Full text available: pdf(146.26 KB) Additional Information: full citation, abstract, references, index terms

This paper deals with the problem of clock skew errors in time-interleaved analog-to-digital converters. Deterministic sample-time errors between time-interleaved channels generate nonlinear distortion and degrade SFDR. We propose a fully digital calibration method that uses, on the one hand, adaptive FIR filters to reconstruct a correctly sampled signal and, on the other hand, a new blind clock skew detection algorithm that guides the adaptive filters. This calibration method applies to any num ...

Keywords: adaptive filters, clock skew, digital calibration, parallel ADC, sample-time errors, time-interleaved

9 TAM Optimization for Mixed-Signal SOCs using Analog Test Wrappers

Anuja Sehgal, Sule Ozev, Krishnendu Chakrabarty

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(167.79 KB) Additional Information: full citation, abstract, citings, index terms

We present a new approach for TAM optimization and testscheduling in the modular testing of mixed-signal SOCs. A testplanning approach for digital SOCs is extended to handle analogcores in a plug-and-play fashion. A test wrapper based on anADC/DAC pair and a digital configuration circuit is designed foranalog cores such that these cores can be accessed through digitalTAMs. In this way, there is no dependence on an analog testbus and expensive mixed-signal testers. Experimental results arepresent ...

10 Supercomputing around the world

A. D. Malony

December 1992 **Proceedings of the 1992 ACM/IEEE conference on Supercomputing**

Full text available: pdf(366.45 KB) Additional Information: full citation, index terms

11 System architectures for computer music

John W. Gordon

June 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 2

Full text available: pdf(4.61 MB) Additional Information: full citation, abstract, references, index terms, review

Computer music is a relatively new field. While a large proportion of the public is aware of

computer music in one form or another, there seems to be a need for a better understanding of its capabilities and limitations in terms of synthesis, performance, and recording hardware. This article addresses that need by surveying and discussing the architecture of existing computer music systems. System requirements vary according to what the system will be used for. Common uses for co ...

12 Concurrent automata, database computers, and security: a "new" security paradigm for secure parallel processing

T. Y. Lin

August 1993 **Proceedings on the 1992-1993 workshop on New security paradigms**

Full text available: pdf(975.78 KB) Additional Information: full citation, abstract, references, citings

Declustering has been proposed to speed up parallel database machines. However, the security requires clustering. In this paper, we use temporal clustering to reconcile the apparent conflict. Automata theory is applied to high level architecture design. Based on Petri net theory a database machine is proposed. The classical notion of clustering is extended to temporal dimension and is imported to parallel database systems. The proposed database machine not only has the linear speedup, ...

13 Closing the gap between analog and digital

Khaled Saab, Naim Ben Hamida, Bozena Kaminska

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(94.67 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a highly effective method for parallel hard fault simulation and test specification development. The proposed method formulates the fault simulation problem as a problem of estimating the fault value based on the distance between the output parameter distribution of the fault-free and the faulty circuit. We demonstrate the effectiveness and practicality of our proposed method by showing results on different designs. This approach extended by parametric fault test ...

Keywords: fault modeling, fault simulation, hard faults, test vector generation

14 Multiplicative Window Generators of Pseudo-random Test Vectors

Janusz Rajski, Jerzy Tyszer

March 1996 **Proceedings of the 1996 European conference on Design and Test**

Full text available: pdf(808.72 KB) Publisher Site Additional Information: full citation, abstract

New arithmetic two-dimensional generators of pseudo-random test vectors are presented. As an integral part of a recently proposed arithmetic built-in self test (ABIST) environment, all generation functions are executed by basic building blocks performing regular functions of data path architectures, yet the scheme is compatible with scan, parallel scan, partial scan and boundary scan designs. The need for extra hardware is either entirely eliminated or drastically reduced, test vectors can be ea ...

Keywords: Accumulators, Arithmetic generators, Built-in self test, Data-path architectures, Pseudo-exhaustive generators, State coverage

15 Numerical stability of algorithms for 2D Delaunay triangulations

Steven Fortune

July 1992 **Proceedings of the eighth annual symposium on Computational geometry**

Full text available: Additional Information: full citation, abstract, references, citings, index

pdf(910.51 KB) terms

We show that two Delaunay triangulation algorithms, a diagonal-flipping algorithm and an incremental algorithm, can be implemented in approxiamte arithmetic. The two algorithms have worst-case running time O(n2) on a set of n sites. The correctness assertion is that the algorithms produce a triangulation of the set of sites so that each triangle has an "almost empty" circumcircle, i.e., a circumscribing pseu ...

16 Mixed-signal design and simulation: A 16-bit mixed-signal microsystem with integrated CMOS-MEMS clock reference

Robert M. Senger, Eric D. Marsman, Michael S. McCorquodale, Fadi H. Gebara, Keith L. Kraver, Matthew R. Guthaus, Richard B. Brown

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(793.60 KB) Additional Information: full citation, abstract, references, citings, index terms

In this work, we report on an unprecedented design where digital, analog, and MEMS technologies are combined to realize a general-purpose single-chip CMOS microsystem. The convergence of these technologies has enabled the development of a low power, portable microinstrument ideally suited for controlling environmental and bio-implantable sensors.

Keywords: ADC, MEMS, PGA, SD, SoC, clock generation, design methodology, inductor, low power, low voltage analog, microcontroller, microsystem, mixed-signal, system-on-chip, varactor

17 A Statistical Approach to Estimate the Dynamic Non-Linearity Parameters of Pipeline ADCs

Mohammad Taherzadeh-Sani, Reza Lotfi, Omid Shoaei

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(402.64 KB) Additional Information: full citation, abstract, index terms

A fully-analytical approach to estimate the statistics ofdynamic non-linearity parameters of pipeline analog-to-digitalconverters (ADCs) in the presence of circuit non-idealitiesincluding capacitance mismatches and non-idealopamps is presented. These parameters include the spurious-freedynamic range (SFDR) and the signal to noise-and-distortionratio (SNDR). The simple closed-form formulasfor SFDR and SNDR presented here are useful for designautomation of highly-linear pipeline ADCs in order toex ...

18 Efficient parallel solution of sparse systems of linear diophantine equations

Mark Giesbrecht

July 1997 **Proceedings of the second international symposium on Parallel symbolic computation**

Full text available: pdf(1.38 MB) Additional Information: full citation, references, citings, index terms

19 A Parallel and Accelerated Circuit Simulator with Precise Accuracy

Peter M. Lee, Shinji Ito, Takeaki Hashimoto, Tomomasa Touma, Hitachi ULSI Systems Co., Junji Sato, Goichi Yokomizo, Semiconductor, Ic, Hitachi, Ltd

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(128.60 KB) Publisher Site Additional Information: full citation, abstract

We have developed a hi ghly parallel and accelerated circuit simulator which produces

precise results for large scale simulation. We incorporated multithreading in both the model and matrix calculations to achieve not only a factor of 10 acceleration compared to the defacto standard circuit simulator used worldwide, but also equal or exceed the performance of timing-based event -driven simulators with the accuracy which matches that of SPICE-based circuit simulation. For example, a 89K element D ...

20 SuperLU_DIST: A scalable distributed-memory sparse direct solver for unsymmetric linear systems

Xiaoye S. Li, James W. Demmel

June 2003 **ACM Transactions on Mathematical Software (TOMS)**, Volume 29 Issue 2

We present the main algorithmic features in the software package SuperLU_DIST, a distributed-memory sparse direct solver for large sets of linear equations. We give in detail our parallelization strategies, with a focus on scalability issues, and demonstrate the software's parallel performance and scalability on current machines. The solver is based on sparse Gaussian elimination, with an innovative static pivoting strategy proposed earlier by the authors. The main advantage of static pivoting o ...

Keywords: Sparse direct solver, distributed-memory computers, parallelism, scalability, supernodal factorization

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1 **A comparative analysis of parallel delta-sigma ADC architectures**
Eshraghi, A.; Fiez, T.S.;
Circuits and Systems I: Regular Papers, IEEE Transactions on [see also Circuit Systems I: Fundamental Theory and Applications, IEEE Transactions on] , Vol 51 , Issue: 3 , March 2004
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